

CLAIMS

What is claimed is:

1. An apparatus comprising:
 - a package including an integrated circuit disposed on two or more electrically coupled die, the first die including a microprocessor and the second die including a memory device;
 - a substrate of the package including one selected from the group consisting of a Land Grid Array, a Pin Grid Array, and a combination thereof electrically coupled to one of the die.
2. The apparatus of Claim 1, further comprising a memory controller electrically coupled to the memory device.
3. The apparatus of Claim 1, further comprising a thin film capacitor integral to the substrate.
4. The apparatus of Claim 1, the second die disposed on a land side of the substrate.
5. The apparatus of Claim 1, further comprising a third die including a second microprocessor, a fourth die including a third microprocessor, and a fifth die including a fourth microprocessor.
6. The apparatus of Claim 5, the second die electrically coupled by one selected from the group including a wirebond electrical interconnect, a flip-chip ball grid array electrical interconnect, a lead frame interconnect, and a combination thereof.
7. The apparatus of claim 1 further comprising a die including one selected from the group including a memory device, a memory controller, an application specific

integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.

8. The memory device of Claim 7 further comprising a fourth level cache.
9. The apparatus of Claim 1, the package further including an integrated heat spreader thermally coupled to one or more of the die.
10. A method comprising:
 - including an integrated circuit disposed on two or more electrically coupled die in a package, the first die including a microprocessor and the second die including a memory device; and
 - electrically coupling a substrate of the package including one selected from the group consisting of a Land Grid Array, a Pin Grid Array, and a combination thereof to at least one of the die.
11. The method of Claim 10, further comprising electrically coupling a memory controller to the memory device.
12. The method of Claim 10 wherein the memory device further comprises a fourth level cache.
13. The method of Claim 10, further comprising integrating a thin film capacitor with the substrate.
14. The method of Claim 10, disposing the second die on a land side of the substrate.

15. The method of Claim 10, further including in the package a third die including a second microprocessor, a fourth die including a third microprocessor, and a fifth die including a fourth microprocessor.
16. The method of Claim 15, the second die electrically coupled by one selected from the group including a wirebond electrical interconnect, a flip-chip ball grid array electrical interconnect, a lead frame interconnect, and a combination thereof.
17. The method of Claim 10, further thermally coupling an integrated heat spreader to one or more of the die.
18. A system comprising:
a package including an integrated circuit disposed on two or more electrically coupled die, the first die including a microprocessor and the second die including a memory device;
a substrate of the package including one selected from the group consisting of a Land Grid Array, a Pin Grid Array, and a combination thereof electrically coupled to at least one of the die; and
a mass storage device coupled to the package.
19. The system of Claim 18 wherein the memory device further comprises a fourth level cache.
20. The system of claim 18, further comprising:
a dynamic random access memory coupled to the integrated circuit; and
an input/output interface coupled to the integrated circuit.
21. The system of claim 20, wherein the input/output interface comprises a networking interface.

22. The system of claim 18, wherein the system is a selected one of a group comprising a set-top box, a media-center personal computer, a digital versatile disk player, a server, a personal computer, a mobile personal computer, a network router, and a network switching device.
23. The system of claim 18, the memory device disposed in a recess formed by a land grid array socket, the package electrically coupled to the land grid array connector.
24. The system of claim 23, the land grid array connector coupled to a printed circuit board assembly capable of further coupling to a motherboard.